

WHAT IS CLAIMED IS:

Sub 1
1. A semiconductor device, comprising:
2 a semiconductor substrate;
3 a gate formed above the semiconductor substrate;
4 an isolation region;
5 at least one of a source/drain region formed above the
6 isolation region.

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6. The semiconductor device as recited in Claim 1 wherein
2 the isolation region extends through a transistor tub.

U.S. Pat. No. 4,340,000

1 7. A semiconductor device, comprising:

2 a channel region located in a semiconductor substrate;
3 a trench located adjacent a side of the channel region;
4 an isolation region located in the trench; and
5 a source/drain region located over the isolation region.

8. The semiconductor device as recited in Claim 7 wherein
2 the isolation region is not located under the channel region.

9. The semiconductor device as recited in Claim 7 wherein
the isolation region comprises an oxide.

10. The semiconductor device as recited in Claim 7 wherein
the source/drain region includes a first portion located in the
semiconductor substrate and a second portion comprising polysilicon
located on the isolation region.

11. The semiconductor device as recited in Claim 7 wherein
2 the isolation region extends through a transistor tub.

Sub A3 → 12. A semiconductor device, comprising:
2 a channel region located in a semiconductor substrate;
3 an isolation region located adjacent the channel region, the
4 isolation region not extending under the channel region; and
5 source/drain regions having a first portion located in the
6 semiconductor substrate and a second portion located on the
7 isolation region.

20 13. The semiconductor device as recited in Claim 12 wherein
the isolation region comprises an oxide.

21 14. The semiconductor device as recited in Claim 12 wherein
the second portion comprises polysilicon.

22 15. The semiconductor device as recited in Claim 12 wherein
the isolation region extends through a transistor tub.

2 16. The semiconductor device as recited in Claim 12 wherein
3 the source/drain regions are first source/drain regions of a first
4 transistor, and the semiconductor device further includes second
5 source/drain regions of a second adjacent transistor, wherein the
6 first source/drain regions are isolated from the second
source/drain regions by the isolation region.

Sub 45
17. A semiconductor device, comprising:

2 a first transistor located adjacent a second transistor,
3 wherein both the first and second transistors are located over a
4 semiconductor substrate;

5 an isolation region located between the first and second
6 transistors; and

7 source/drain regions associated with each of the first and
8 second transistors, each of the source/drain regions having a first
9 portion located in the semiconductor substrate and a second portion
10 located on the isolation region.

18. The semiconductor device as recited in Claim 17 wherein
2 the isolation region comprises an oxide.

19. The semiconductor device as recited in Claim 17 wherein
2 the second portion comprises polysilicon.

20. The semiconductor device as recited in Claim 17 wherein
2 the isolation region extends through a transistor tub.

SUB 5 → 21. A method of manufacturing a semiconductor device,
comprising:

2
3 providing a semiconductor substrate;
4 creating a gate above the semiconductor substrate;
5 forming an isolation region;
6 forming at least one of a source/drain region above the
7 isolation region.

22. The method as recited in Claim 21 wherein forming an
isolation region includes forming an isolation region adjacent to
the semiconductor region.

23. The method as recited in Claim 21 wherein forming an
isolation region includes forming an isolation region that is not
located under a channel region.

24. The method as recited in Claim 21 wherein forming an
isolation region includes forming an oxide isolation region.

SUB B8 → 25. The method as recited in Claim 21 wherein forming the at
least one source/drain region includes forming a portion of the at
least source/drain region with polysilicon.

26. The method as recited in Claim 21 wherein forming an
isolation region includes forming an isolation region that extends
through a transistor tub.

Sub 16 → 27. An integrated circuit, comprising:
2 semiconductor devices including;
3 a semiconductor substrate;
4 a gate formed above the semiconductor substrate;
5 an isolation region;
6 at least one of a source/drain region formed above the
7 isolation region; and
8 interconnect structures contacting the semiconductor devices.

28. The integrated circuit as recited in Claim 27 wherein the
isolation region is formed adjacent the semiconductor substrate.

29. The integrated circuit as recited in Claim 27 wherein the
isolation region is not located under a channel region.

30. The integrated circuit as recited in Claim 27 wherein the
isolation region comprises an oxide.

SUB B10 → 31. The integrated circuit as recited in Claim 27 wherein a
2 portion of the at least one source/drain region comprises
3 polysilicon.

32. The integrated circuit as recited in Claim 27 wherein the

2 isolation region extends through a transistor tub.

33. The integrated circuit as recited in Claim 27 further
2 including additional active and passive devices.